particular attention to the points raised in the Office Action. It is submitted that no new matter has been added and no new issues have been raised by the present Amendment.

Attached hereto is a version with markings to show changes made to the Claims by the current Amendment.

Reconsideration is respectfully requested of the objection to the Abstract of the Disclosure. In response to the objection by the Examiner, the Abstract of the Disclosure has been corrected.

Reconsideration is respectfully requested of the objection to the Specification. In response to the objections by the Examiner, the Specification has been corrected.

Reconsideration is respectfully requested of the rejection of claims 1, 3, and 16 under 35 U.S.C. § 112, second paragraph, as allegedly containing subject matter which was not described in the Specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The instances noted by the Examiner have been corrected in the amendments made to the Specification and to the Claims hereby. The Specification has been amended to clarify that the low pass filter described in the section of the Specification entitled "Background of the Invention" is a conventional low pass filter. Furthermore, the phrase "increase and decrease" means has been amended in light of the comments made by the Examiner.

Reconsideration is respectfully requested of the rejection of claims 1-18 under 35 U.S.C. § 112, second paragraph, as allegedly being vague and indefinite. The

instances noted by the Examiner have been corrected in the amendments made to the Claims hereby.

Withdrawal of the rejections under 35 U.S.C. § 112, second paragraph, is respectfully requested.

Reconsideration is respectfully requested of the rejection of claims 1-2, 6, 8-9, and 12-13 under 35 U.S.C. § 103(a), as being allegedly unpatentable over U.S. Patent No. 5,140,245 (Stacey) in view of U.S. Patent No. 5,734,172 (Pryor et al.) and U.S. Patent No. 5,432,443 (Maejima et al.).

Applicants have carefully considered the Examiner's comments and the cited reference, and respectfully submit that claims 1-2, 6, 8-9, and 12-13 are patentably distinct over the cited reference for at least the following reasons.

The present invention relates to a position detection apparatus for detecting a position of movement of two members that move relative to one another and to an arithmetic processing unit for position detection. The position detection apparatus contains a recording medium, a detection section including first and second detection heads, a polar conversion section, a low pass filter, and an output section. The position detection apparatus removes a noise component from an angle signal obtained by performing polar conversion with respect to a position signal.

Stacey, as understood by Applicants, relates to a permanent magnet generator (PMG)-based position sensor and synchronous drive incorporating the sensor. A PMG is driven by a rotating shaft and generates a multiphase output that is integrated and applied as an input to a high resolution phase locked loop having a binary counter with an output phase

locked to the PMG multiphase output and representing a shaft position. The digital shaft position signal is used to generate a multiphase current reference signal that is tracked by stator currents generated for the synchronous machine by a power current source.

The Examiner notes that Stacey does not disclose a conversion of a position signal into polar coordinates or a detection section including two detection heads for reading a periodic position signal (see Office Action, p. 8, lns. 9-13). Pryor et al. and Maejima et al. are apparently cited to show these missing elements.

Pryor et al., as understood by Applicants, apparently relates to a method and apparatus for electro-optically determining the dimension, location, and attitude of objects. Particular embodiments include optical triangulation-based coordinate measurement machines capable of accurate measurement of complex surfaces such as gear teeth and turbine blades.

Maejima et al., as understood by Applicants, apparently relates to a linear position detector including a phase shifter and a sample-and-hold circuit for synchronizing a sample pulse period with the reference period of the equilibrium modulated signal. The equilibrium modulated signal is derived from at least one detecting head and is processed and converted into a DC voltage signal. A level of the DC voltage signal indicates a relative displacement of a scale to the head.

It is respectfully submitted that the sensor configuration of Pryor et al. (see Pryor et al., col. 7, lns.

46-60) relates to the measurement of surface features of an object being measured, and does not suggest or disclose a polar conversion section for converting a position signal detected by a first detection head and a second detection head into an angle signal that represents a relative position of a recording medium and a detection section as an angle, as recited in the present application.

Furthermore, it is respectfully submitted that none of the cited references, alone or in combination, suggest or disclose the passing of angle data obtained by polar conversion of a position signal through a specially constructed low pass filter to enable accurate filtering, as recited in the present application.

Accordingly, for at least the above-stated reasons, it is respectfully submitted that amended independent claim 1, and the claims depending therefrom, are patentable over Stacey in view of Pryor et al. and Maejima et al.

Reconsideration is respectfully requested of the rejection of claims 7, 10, and 11 under 35 U.S.C. § 103(a), as being allegedly unpatentable over Stacey in view of Pryor et al. and Maejima et al., and further in view of U.S. Patent No. 5,526,332 (Yamada et al.).

Applicants have carefully considered the Examiner's comments and the cited reference, and respectfully submit that claims 7, 10, and 11 are patentably distinct over the cited reference for at least the following reasons.

Yamada et al., as understood by Applicants, relates to a reference clock generator for a sampled servo type disk unit and a disk unit. In a reference clock signal generator for

generating a sampled servo format reference clock signal using a PLL circuit, a unique distance is detected by an output signal of a VCO in a state the PLL circuit is operated based on a clock signal which corresponds to a number of rotations of a disk in generating the reference clock signal. When the distance is detected a dividing ratio of a frequency divider is changed to operate the PLL circuit based on a clock mark detecting signal. The dividing ratio is set so that an oscillation frequency of the VCO becomes constant before and after switching from the clock signal that corresponds to the number of rotations of the disk to the clock mark signal. A count of the frequency divider is preset to zero with the first clock mark signal after the detection of the unique distance and the detection of the clock marks thereafter is carried out based on the count of the frequency divider.

It is respectfully submitted that Yamada et al. does not suggest or disclose the passing of angle data obtained by polar conversion of a position signal through a specially constructed low pass filter to enable accurate filtering, as recited in the present application. Therefore, for at least the reasons stated above, it is further submitted that combining Yamada et al. with Stacey, Pryor et al., and Maejima et al. does not disclose or suggest the polar conversion, angle data, and low pass filter features as recited in the present application.

Accordingly, for at least the above-stated reasons, it is respectfully submitted that amended independent claim 1, and the claims depending therefrom, are patentable over Stacey in view of Pryor et al. and Maejima et al., and further in view

of Yamada et al.

Reconsideration is respectfully requested of the rejection of claims 7, 10, and 11 under 35 U.S.C. § 103(a), as being allegedly unpatentable over Stacey in view of Pryor et al. and Maejima et al., and further in view of U.S. Patent No. 5,852,413 (Bacchi et al.).

Applicants have carefully considered the Examiner's comments and the cited reference, and respectfully submit that claims 7, 10, and 11 are patentably distinct over the cited reference for at least the following reasons.

Bacchi et al., as understood by Applicants, relates to a virtual absolute position encoder. A rotary stage is positionable in precise angular increments that are determined by a virtual absolute position encoder disk. The angular increments are determined to a 2,400 arc-second absolute resolution by a bar code scale and to a 0.125 arc-second relative resolution by interpolating interference patterns generated by a diffraction grating-based incremental encoder scale.

It is respectfully submitted that Bacchi et al. does not suggest or disclose the passing of angle data obtained by polar conversion of a position signal through a specially constructed low pass filter to enable accurate filtering, as recited in the present application. Therefore, for at least the reasons stated above, it is further submitted that combining Bacchi et al. with Stacey, Pryor et al., and Maejima et al. does not disclose or suggest the polar conversion, angle data, and low pass filter features as recited in the present application.

Accordingly, for at least the above-stated reasons, it is respectfully submitted that amended independent claim 1, and the claims depending therefrom, are patentable over Stacey in view of Pryor et al. and Maejima et al., and further in view of Bacchi et al.

Reconsideration is respectfully requested of the rejection of claims 16 and 17 under 35 U.S.C. § 103(a), as being allegedly unpatentable over Stacey in view of Pryor et al. and Maejima et al., and further in view of allegedly "admitted prior art."

The alleged "admitted prior art" cited above is not seen to disclose the polar conversion, angle data, and low pass filter features as recited in the present application. Furthermore, for at least the reasons detailed above, it is respectfully submitted that combining Stacey, Pryor et al., and Maejima et al. does not disclose or suggest the polar conversion, angle data, and low pass filter features as recited in the present application. Therefore, it is respectfully submitted that amended independent claim 16, and the claim depending therefrom, are patentable over the cited references.

Should the Examiner disagree, it is respectfully requested that the Examiner specify where in the cited document there is a basis for such disagreement.

The references cited as of interest have been reviewed and are not seen to show or suggest the present invention, as recited in the amended claims.

The Office is hereby authorized to charge any additional fees which may be required in connection with this Amendment

and to credit any overpayment to Deposit Account No. 03-3125.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,
COOPER & DUNHAM, LLP

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JHM/AVF

VERSION WITH MARKINGS TO SHOW CHANGES MADE ✓

IN THE ABSTRACT OF THE DISCLOSURE

The Abstract of the Disclosure has been amended as follows:

--[A noise component is removed from an angle signal obtained by performing polar conversion with respect to a position signal.] Angle data [PI in the range of 0] ranging from 0° to 360° obtained by performing polar conversion with respect to a periodic signal [is] are input to a low pass filter [7. The low pass filter 7 has] having: a [VCO 36] phase accumulator for outputting smoothed angle data [PF]; a phase comparator [31] for obtaining a phase error [PE] between the angle data [PI] and the smoothed angle data [PF]; a first amplifier [32] for amplifying the phase error [PE]; a second amplifier [33] for further amplifying the phase error [PE amplified by the first amplifier 32]; an integrator [34] for integrating the phase error PE amplified by the second amplifier [33] to obtain a velocity error [VEL]; and an adder [35] for adding the phase error [PE] amplified by the first amplifier [32] and the velocity error [VEL] to determine a control voltage [VS]. The [VCO 36] phase accumulator controls the frequency of the smoothed angle data [PF] so that the phase error is zero based on the control voltage [FS,] to remove a high frequency component in the [input] angle data [PI].--

IN THE SPECIFICATION

The paragraph beginning on page 2, line 11 has been amended as follows:

--With a conventional position detection apparatus, it is necessary to provide a low pass filter in order to remove internal noise such as detection noise by means of the head section, quantization noise at the time of A/D conversion, quantization noise at the time of polar conversion or the like. However, when the conventional low pass filter is [directly] applied to the angle signal, filtering cannot be performed precisely. For example, if a portion jumping from 360° up to 0° is smoothed, the conventional low pass filter regards the smoothed portion as an angle change from 360° up to 0°, hence, the output thereof is a value in the vicinity of 180° on the contrary, as shown in Fig. 2.--

The paragraph beginning on page 16, line 20 has been amended as follows:

--Moreover, though the first position detection head 15 and the second position detection head 16 are arranged so as to effect a phase shift by 1/4 wavelength in the detected signal, these may be arranged so as to effect the phase shift not only by 1/4 wavelength but also by other phase value, since with the position detection apparatus 1, a position in one period of the position signal has only to be specified by an angle, from two signals detected by the polar conversion

section [5] 6 described later.--

The paragraph beginning on page 43, line 20 has been amended as follows:

--The response limiting section 10 has a first subtractor 70, an absolute value conversion circuit 71, a second subtractor 72, a multiplexer 73, a through rate generating circuit 74, a comparator [7T] 75, an absolute value inverse circuit 76, an adder 77 and a latch 78.--

The paragraph beginning on page 54, line 16 has been amended as follows:

--As shown in Fig. 31, 24-bit in-quadrant division unit address PDL (PDL0-PDL23) are output from the first multiplier 81. From the [third [second]] second multiplier 82, 4-bit correction address PC ((PH14, PH15)*(DivL0, DivL1) = PC14, PC15, PC16, PC16) is output. Then, the correction adder 83 adds the lower 2 bits of the correction address PC and the upper tenth bit and eleventh bit (PDL14, PDL15) of he 24-bit in-quadrant division unit address PDL, to thereby output one wavelength division unit address AD (AD0, AD1).--

IN THE CLAIMS

Claims 1-5, 9-10, 12-14, and 16-17 have been amended as follows:

--1. (Twice Amended) A position detection apparatus comprising:

a recording medium on which a periodic position signal [having a periodic signal] is recorded;

a detection section having a first detection head [which] that moves relative to said recording medium along a recording direction of said position signal for detecting said position signal[,] and a second detection head disposed apart from said first detection head by a predetermined distance along said recording direction of said position signal [which] that moves relative to said recording medium[, operating] and that operates with said first detection head for detecting said position signal;

a polar conversion section for converting said position signal detected by said first detection head and said second detection head into an angle signal [representing] that represents a relative position of said recording medium and said detection section [in one period] as an angle;

a low pass filter for removing a high [pass] frequency component in said angle signal output from said polar conversion section to output an angle signal having a frequency such that a phase error is zero; and

an output section for outputting relative position information of said recording medium and said detection section[,] based on said smoothed angle signal from which said high [pass] frequency component has been removed by said low pass filter.

--2. (Twice Amended) The position detection apparatus according to claim 1, wherein said low pass filter comprises:

a frequency control oscillator for outputting a periodic

signal having a frequency controlled based on a frequency control signal;

a phase comparator for comparing a phase of said angle signal output from said polar conversion section and said periodic signal output from said frequency control oscillator to output [a] said phase error;

first gain-controllable amplifier means for one of increasing and decreasing said phase error output from said phase comparator;

second gain-controllable amplifier means for one of increasing and decreasing said phase error output from said first amplifier means;

an integrator for integrating said phase error output from said [phase comparator] second gain-controllable amplifier means to output a velocity error; and

an adder for adding said velocity error output from said integrator and said phase error output from said [phase comparator] first gain-controllable amplifier means to generate said frequency control signal,

wherein said frequency control oscillator controls said frequency of said periodic signal such that said phase error is zero based on said frequency control signal[,] and outputs said periodic signal as said smoothed angle signal from which said high [pass] frequency component has been removed.

--3. (Twice Amended) The position detection apparatus according to claim 2, wherein said [low pass filter comprises:

first increase and decrease means for increasing or decreasing said phase error output from said phase comparator;

and

second increase and decrease means for increasing or decreasing said phase error output from said first increase and decrease means,

wherein said] integrator integrates said phase error increased or decreased by said second [increase and decrease] gain-controllable amplifier means; and

said adder adds said velocity error output from said integrator and said phase error output from said [increase and decrease] first amplifier means.

--4. (Twice Amended) The position detection apparatus according to claim 2, further comprising a prediction section having [an] a prediction section adder [which] that adds said velocity error output from said integrator in said low pass filter and said smoothed angle signal output from said frequency control oscillator,

wherein said output section outputs said relative position information of said recording medium and said detection section, based on a signal output from said prediction section.

--5. (Twice Amended) The position detection apparatus according to claim 4, wherein said prediction section has third [increase and decrease] gain-controllable amplifier means for increasing or decreasing said velocity error output from said integrator in said low pass filter[,

wherein] ; and said prediction section adder adds said smoothed angle signal output from said frequency control

oscillator and a velocity error output from said third [increase and decrease] amplifier means.

--9. (Twice Amended) The position detection apparatus according to claim 8, wherein said gain control section controls said gain of said phase error output from said phase comparator[, depending] based on a size of said phase error and/or a frequency of said phase error.

--10. (Twice Amended) The position detection apparatus according to claim 8, [wherein] said polar conversion section [generates] generating an amplitude signal together with said angle signal[,] and [comprises] comprising:

a noise detection section for detecting inside noise based on said amplitude signal and/or said phase error,

wherein said gain control section decreases said gain of said phase error output from said phase comparator[,] when external noise occurs[,] or said noise detection section detects noise.

--12. (Twice Amended) The position detection apparatus according to claim 8, wherein said gain control section decreases said gain of said phase error[,] when an absolute value of said phase error output from said phase comparator [increases, exceeding] exceeds a predetermined level.

--13. (Twice Amended) The position detection apparatus according to claim 12, wherein said gain control section decreases said gain of said phase error[,] when said condition

that said absolute value of said phase error output from said phase comparator [increases, exceeding] exceeds said predetermined level for a predetermined time.

--14. (Twice Amended) The position detection apparatus according to claim 1, wherein said polar conversion section designates said position signal detected by said first detection head and said second detection head as an address, and uses a table [wherein] within which said angle signal corresponding to said address is stored[,] to generate said angle signal representing said relative position of said recording medium and said detection section [in one period] as said angle.

--16. (Twice Amended) An arithmetic processing unit comprising:

a polar conversion section for converting a first periodic signal and a second periodic signal whose phase is different from that of said first periodic signal into an angle signal showing an angle [in one period] of said first periodic signal and said second periodic signal;

a low pass filter for removing a high [pass] frequency component in said angle signal output from said polar conversion section to output an angle signal having a frequency such that a phase error is zero; and

an output section for outputting position information shown by said first periodic signal and said second periodic signal, based on said angle signal from which said high [pass] frequency component has been removed by said low pass filter.

--17. (Twice Amended) The arithmetic processing unit according to claim 16, wherein said low pass filter comprises:

a frequency control oscillator for outputting a periodic signal having a frequency controlled based on a frequency control signal;

a phase comparator for comparing a phase of said angle signal output from said polar conversion section and said periodic signal output from said frequency control oscillator to output [a] said phase error;

an integrator for integrating said phase error output from said phase comparator to output a velocity error; and

an adder for adding said velocity error output from said integrator and said phase error output from said phase comparator to generate said frequency control signal,

wherein said frequency control oscillator controls said frequency of said periodic signal such that said phase error is zero based on said frequency control signal, and outputs said periodic signal as said angle signal from which said high [pass] frequency component has been removed.--